MOTOROLA

MC2800SYNEVK

Advance Information

FLEX™ Paging RF/IF Frequency Synthesizer Receiver

This document contains the information of a frequency synthesized receiver prototype for FLEX roaming paging platform. This FLEX paging receiver board is a high performance RF/IF front–end for using in FLEX roaming pager. This board employs Motorola's high frequency transistors MMBR941LT1, a M–ary FSK FM IF receiver MC2800 as well as NPC's phase lock loop SM5166AV as the core. The whole module includes a LNA, a voltage–controlled oscillator, a frequency multiplier, a PLL, a mixer and a FSK IF receiver.

Features:

- Input RF Frequency Range: 278 to 286 MHz
- Input frequency channel spacing: 25.0 kHz
- Excellent Sensitivity: –123.0 dBm
- IF Receiver Operating Voltage: 1.15 to 1.7 V
- PLL Operating Voltage: 3.0 to 3.3 V
- Total Current Consumption:
  4.3 mA @ V_{CC} = 1.15 V,
  0.08 mA @ V_{DD} = 3.0 V
- Switchable Bit–Rate Filter to Support All Kinds of FLEX Data Rate

ORDERING INFORMATION

Device	Description
MC2800SYNEVK	FLEX Paging Receiver Brd Evaluation Kit

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Figure 1. System Block Diagram

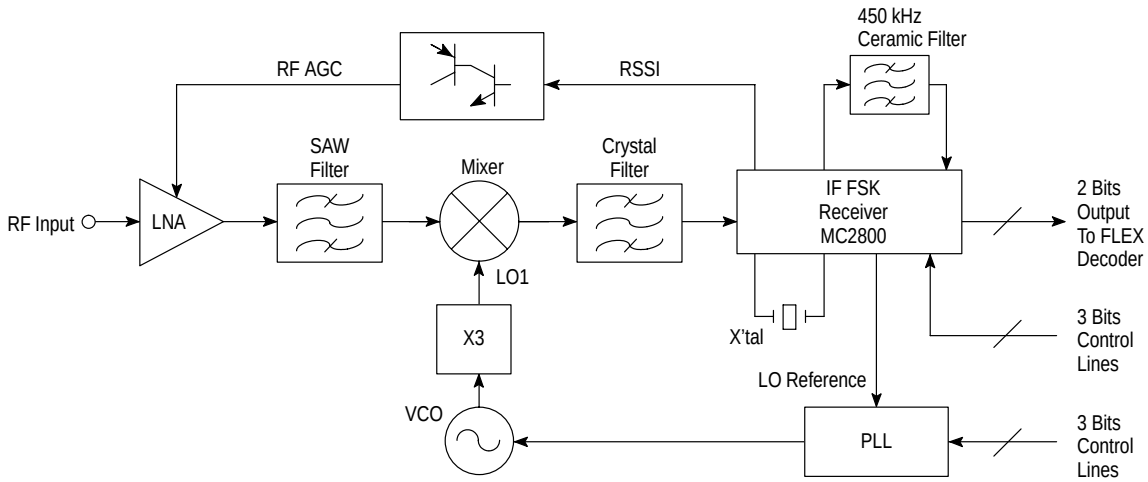
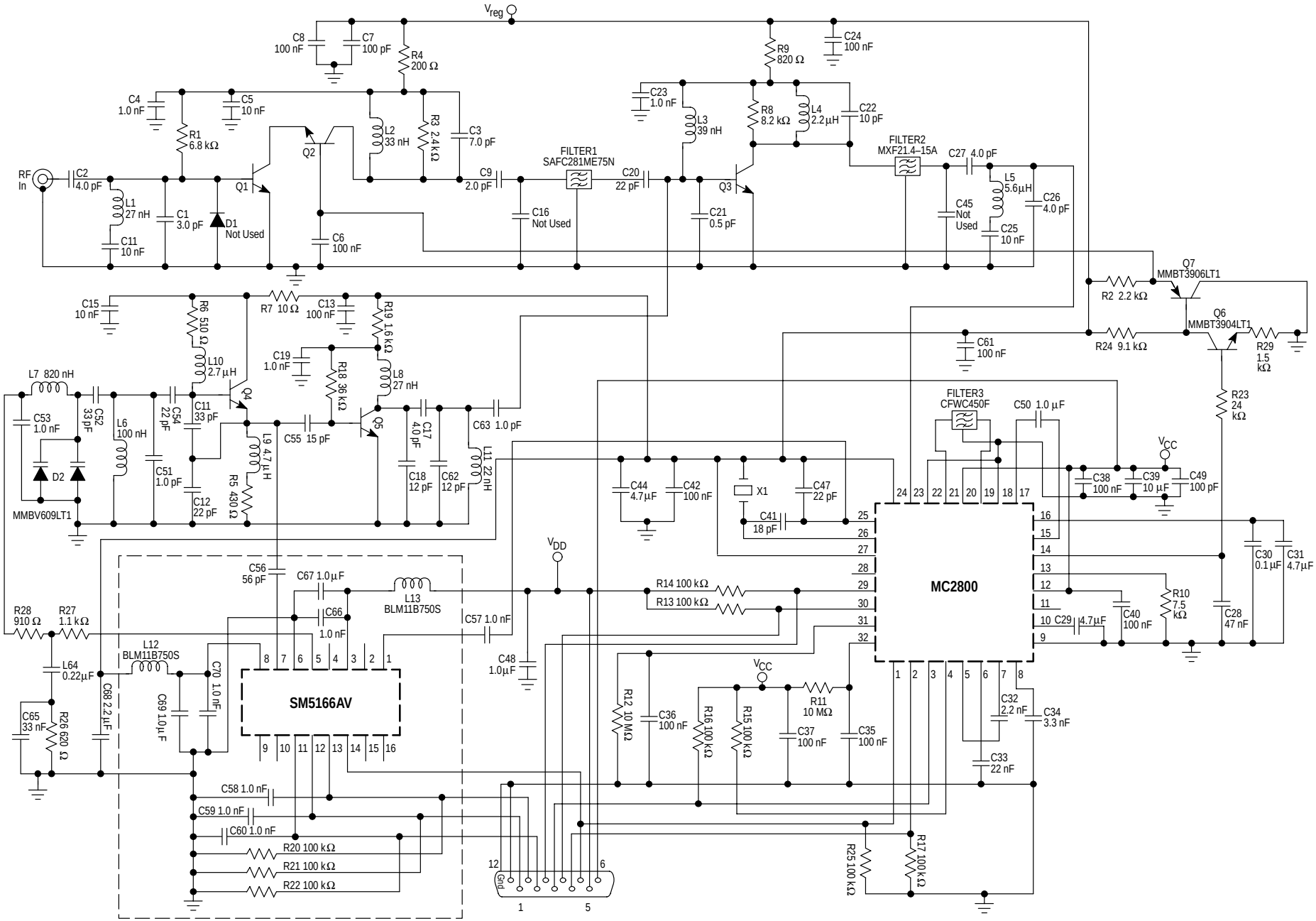


Figure 2. The Schematic of the Frequency Synthesized RF/IF Receiver Board



RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Operating Voltage	V_{CC}	1.15	–	1.7	V
RF Input Frequency Range		278	–	286	MHz
PLL & FLEX Decoder Interface Voltage	V_{DD}	3.0	–	3.3	V

TEST CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Operating Voltage	V_{CC}	–	1.15	–	V
PLL & FLEX Decoder Interface Voltage	V_{DD}	–	3.3	–	V
MC2800 Regulated Output Voltage	V_{reg}	–	0.980	–	V
RF Input Frequency	f_{RF}	–	282.0000	–	MHz
Synthesizer Frequency	f_{syn}	–	260.6000	–	MHz

ELECTRICAL CHARACTERISTICS

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
LOW NOISE AMPLIFIER						
Power Gain [Note 1]	@ 282.000 MHz	G_P	–	19.9	–	dB
S11 [Note 1]		S_{11}	–	–10.1	–	dB
Zout [Note 1]		Z_{out}	–	227 + j46	–	Ω
Noise Figure [Note 1]		NF	–	3.3	–	dB
Current Consumption	V_{reg} = 0.980 V	I	–	850	–	μA
SAW FILTER						
Insertion Loss	Terminating Impedance = 230 Ω		–	1.0	–	dB
VOLTAGE CONTROLLED OSCILLATOR + FREQUENCY MULTIPLIER						
Desired Output Tone Frequency	3rd Harmonic	f_{LO1}	–	260.6008	–	MHz
Desired Output Tone Amplitude		V_{LO}	–	53	–	mV
2nd Harmonic Output Power	Referenced to 3rd Harmonic	H2	–	–46	–	dBc
4th Harmonic Output Power		H4	–	–31	–	dBc
Current Consumption	V_{reg} = 0.980 V	I	–	1050	–	μA
FREQUENCY SYNTHESIZER						
Reference Frequency		f_{ref}	–	20.95008	–	MHz
Reference Counter (R–Counter)		–	–	$09D2_{(H)}$	–	
Channel Spacing		f_{ch}	–	25.000	–	kHz
N–Counter Range		N	$2810_{(H)}$	–	$2950_{(H)}$	
Synthesizer Frequency Range		f_{syn}	256.600	–	264.600	MHz
Phase Noise @ 10kHz Offset	N = $28B0_{(H)}$ fsyn = 260.600 MHz	–	–	–95	–	dBc / Hz
V_{CC} Current Consumption of PLL	V_{reg} = 0.980 V	I	–	750	–	μA
V_{DD} Current Consumption of PLL	V_{DD} = 3.3 V	I	–	70	–	μA

NOTES: 1. Output of the LNA is matched to 230 Ω by inserting a 180 Ω resistor in series with its output port.
2. Output of the Mixer is matched to 1.5050 kΩ by inserting a 1500 Ω resistor in series with its output port.
3. The circuit of this test board is the same as the schematic in Figure 2.

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
LNA + SAW FILTER + MIXER						
Conversion Gain [Note 2]	Input @ 282.000 MHz Output @ 21.400 MHz	G_C	–	28.2	–	dB
Zout	@ 21.400 MHz	Z_{out}	–	1620 – j51	–	Ω
Current Consumption of Mixer	V_{reg} = 0.980 V	I	–	370	–	μA
CRYSTAL FILTER						
Insertion Loss	Terminating Impedance = 1.5 kΩ		–	1.0	–	dB
IF RECEIVER MC2800						
Input Impedance	@ 21.400 MHz	Z_{in}	–	1090 – j140	–	Ω
Second Local Oscillator Frequency		f_{LO2}	–	20.95008	–	MHz
Startup Time of 2nd LO	EN transits from '0' to '1'		–	<1.0	–	ms
Current Consumption	V_{CC} = 1.15 V		–	1.45	–	mA
OVERALL RECEIVER PERFORMANCE (a) Phase A Characteristics [Note 3]						
RF Input Frequency	N – Counter = $28B8_{(H)}$		–	282.000	–	MHz
Sensitivity 6400/4 Level FSK 1600/2 Level FSK	 R1 = '0' R1 = '1'		 – –	 –123 –123	 – –	 dBm dBm
Co–channel Rejection	6400/4 Level FSK R1 = '0'		–	–5.0	–	dB
Adjacent Channel Rejection Low Side High Side			 – –	 56 59	 – –	dB
Image Rejection First IF Second IF			 – –	 56 51	 – –	dB
Intermodulation Rejection Low Side High Side			 – –	 52 52	 – –	dB
Blocking @ 1.0 MHz @ 5.0 MHz			 – –	 73 78	 – –	dB
Total Current Consumption Power Up Power Down	 @ V_{CC} = 1.15 V @ V_{CC} = 1.15 V		 – –	 4.3 10	 – –	 mA μA

NOTES: 1. Output of the LNA is matched to 230 Ω by inserting a 180 Ω resistor in series with its output port.
2. Output of the Mixer is matched to 1.5050 kΩ by inserting a 1500 Ω resistor in series with its output port.
3. The circuit of this test board is the same as the schematic in Figure 2.

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
(b) Phase B Characteristics [Note 3]						
RF Input Frequency	N – Counter = $28B8_{(H)}$		–	282.000	–	MHz
Sensitivity						
6400/4 Level FSK	R1 = '0'		–	–119	–	dBm
1600/2 Level FSK	R1 = '1'		–	–119	–	dBm
Co–channel Rejection	6400/4 Level FSK R1 = '0'		–	–10	–	dB
Adjacent Channel Rejection						dB
Low Side			–	56	–	
High Side			–	56	–	
Image Rejection						dB
First IF			–	53	–	
Second IF			–	50	–	
Intermodulation Rejection						dB
Low Side			–	47	–	
High Side			–	48	–	
Blocking						dB
@ 1.0 MHz			–	69	–	
@ 5.0 MHz			–	67	–	
Total Current Consumption						
Power Up	@ V_{CC} = 1.15 V		–	4.3	–	mA
Power Down	@ V_{CC} = 1.15 V		–	10	–	µA

NOTES: 1. Output of the LNA is matched to 230 Ω by inserting a 180 Ω resistor in series with its output port.
2. Output of the Mixer is matched to 1.5050 kΩ by inserting a 1500 Ω resistor in series with its output port.
3. The circuit of this test board is the same as the schematic in Figure 2.

PIN FUNCTION DESCRIPTION

Pin	Symbol	Description
1	PLL_DATA	PLL serial data input.
2	PLL_CLOCK	PLL clock signal.
3	R1	Control bit of the MC2800 bit–rate filter. Default value = '1'.
4	RESET	Pre–charge and reset of the MC2800. Default value = '0'.
5	V_{DD}	Digital part of PLL and FLEX decoder operating voltage.
6	V_{CC}	Battery supplies of MC2800.
7	ENABLE	MC2800 & PLL enable pin. (Vdd when 'ON')
8	D2	2–bit digital outputs of the MC2800.
9	D1	2–bit digital outputs of the MC2800.
10	PLL_LATCH	PLL input data latch.
11	Gnd	Ground pin.

This frequency synthesized FLEX paging receiver board uses Motorola's NPN silicon low–noise high–frequency transistors MMBR941LT1 to construct the RF functional blocks, including a LNA, a voltage controlled oscillator (VCO), a frequency multiplier and a mixer. NPC's PLL IC SM5166AV is used as the core of the fractional–N synthesizer. The varactor diode MMBV609LT1 is used in the VCO. The M–ary FSK IF receiver MC2800 performs the second down–conversion and demodulates the received FSK signal into two digital output bits for the baseband. Two general purpose NPN & PNP BJTs, MMBT3904LT1 & MMBT3906LT1 form the RSSI to RF AGC conversion circuit.

The LNA employs cascode architecture (Q1 and Q2) with its output being matched to 230 , the input impedance of the 281–MHz SAW filter. The gain of the LNA is controlled by the base voltage of Q2, which is a function of the RSSI output of MC2800. The input matching network should be changed when an antenna precedes the LNA. Special care must be taken in characterizing the LNA and antenna to achieve a good interface match.

The frequency synthesizer comprises a VCO, a NPC's PLL IC SM5166AV, a loop filter and a frequency multiplier. The VCO (Q4) uses a modified Colpitts structure with a varactor diode D2 for the frequency tuning. C52 can be adjusted to change the frequency tuning range. The PLL uses an input reference frequency of 20.950 MHz with a divider value of 2514 (decimal), which results in a frequency spacing of 8.333 kHz. The pre–scalar value of the PLL has a control range from 10256 to 10576 (decimal). The loop filter consisting of R26, R27, C64 & C65 has a bandwidth of about 1/10 to 1/15 of the frequency spacing. Q5 is used for frequency multiplication with a ratio of 3. The third harmonic is extracted by the bandpass filter formed by C16, C17, C62, C63 & L11. This results in a synthesized frequency range from 256.600 to 264.600 MHz. For the details of the control of PLL IC, please refer to the data sheet of SM5166AV.

A common emitter circuit (Q3) is used as the mixer with both LO and RF being ac–coupled to its base. Its output is dc–coupled to the 21.4–MHz crystal filter. To minimize the distortion of the downconverted frequency spectrum, the filter output must be matched to MIX_IN of the MC2800.

For the characteristics of the MC2800 as well as its control (ENABLE & RESET pins) and bit–rate filter (R1 pins) setup, please refer to the MC2800 data sheet. It is recommended that a single ceramic filter configuration be used. That is, a 450–kHz filter (FILTER3 in Figure 2) is inserted between the MIX_OUT and IF1_IN, and a 1.0 F multi–layer ceramic chip capacitor (C73 in Figure 2) is connected between the IF1_OUT and IF2_IN. Although it is noted in the data sheet of MC2800 that 3.0 to 4.0 dB performance degradation is observed in the single ceramic filter application, this performance degradation does not occur in the overall RF/IF system performance. This is because the high gain and the low NF of the RF front–end have effectively reduced the noise contribution of the MC2800 to the overall system.

FDB Interface

This pager board uses an 11–pin surface mount socket to interface with the pager baseband board. This interface provides 2 digital output pins (D1 & D2), 6 control pins (ENABLE, RESET, R1, PLL_DATA, PLL_CLOCK & PLL_LATCH) and 3 supply pins (VCC, VDD & GND). The pin descriptions are summarized in the following table and the footprint of this socket is depicted in Figure 3. In order to provide default states for these input pins, a pull up resistor (R16) is used at R1 input pin whereas pull down resistors (R17, R20, R21, R22 & R25) are connected at the rest of input pins.

Note: For general information regarding FLEX products, please contact the local Motorola SPS sales office or the web at **http://www.motorola.com/wireless–semi**.

Figure 3. The Footprint of the 11 Pin Interface Socket

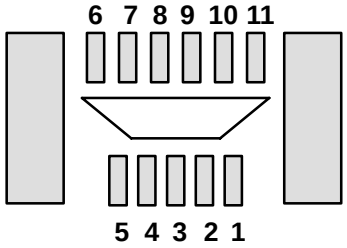


Figure 4. The PCB Layout of the Receiver Board (Top Layer)

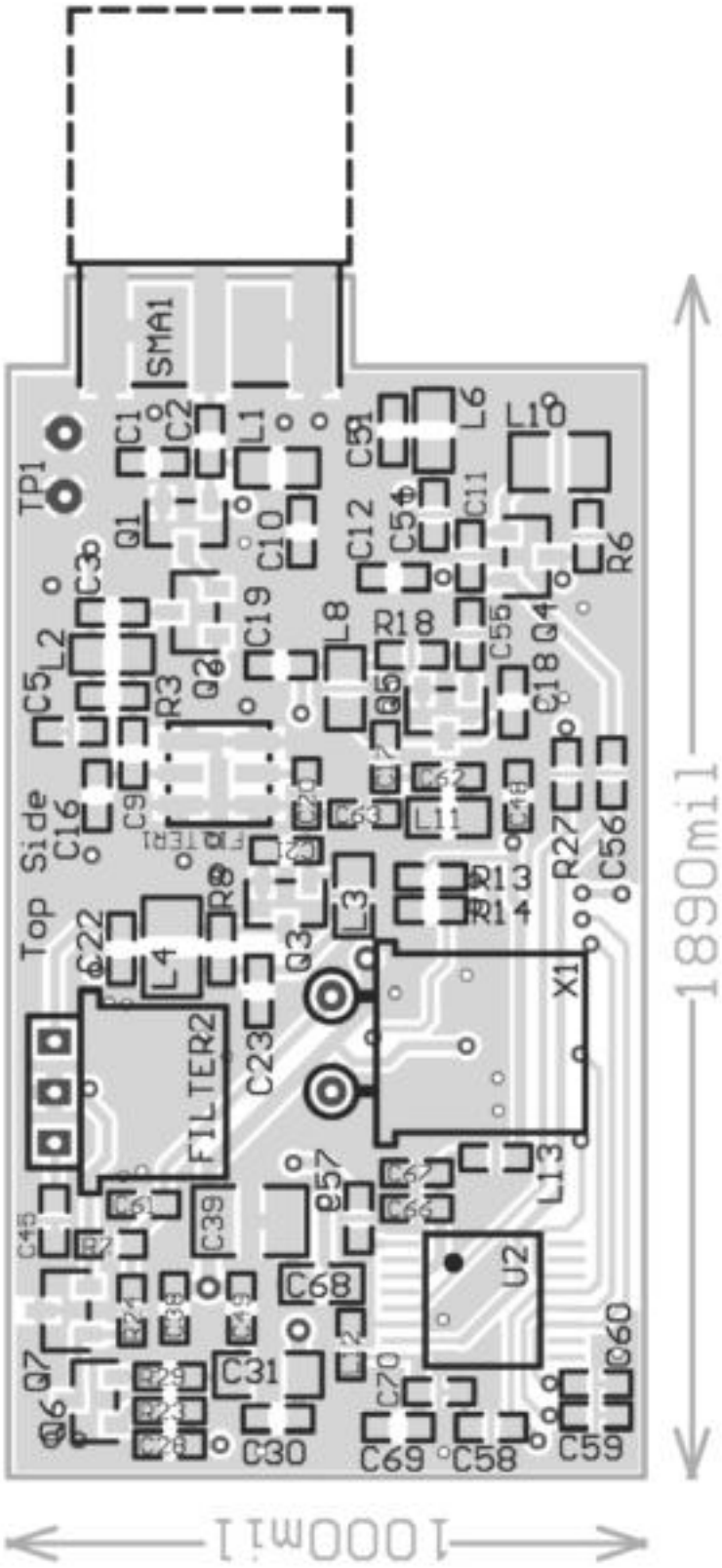


Figure 5. The PCB Layout of the Receiver Board (Bottom Layer)

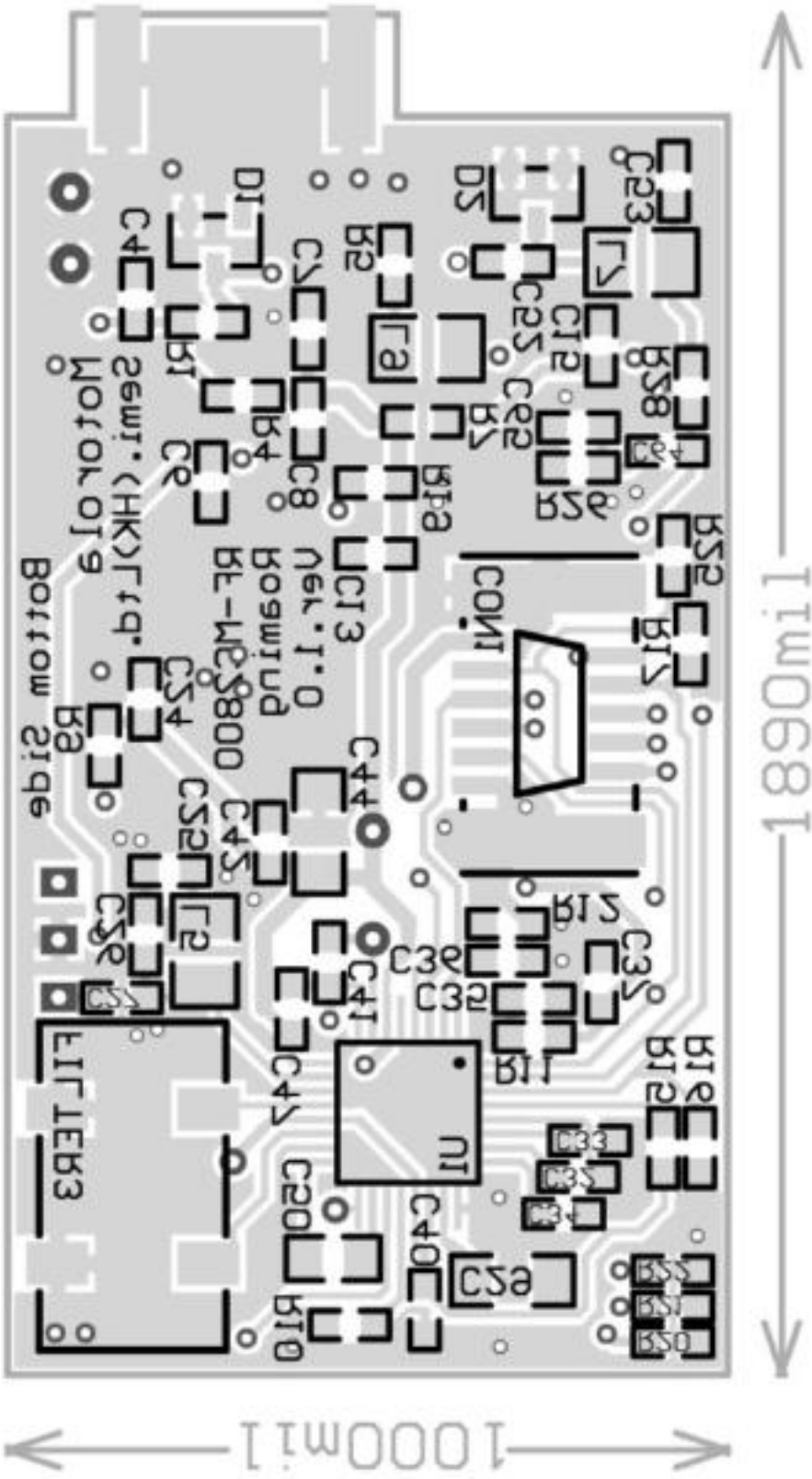


Table 1. Component List

C1	3.0 pF	L3	39 nH
C2, C17, C26, C27	4.0 pF	L4	2.2 µH
C3	7.0 pF	L5	5.6 µH
C4, C19, C23, C53, C57, C58, C59, C60, C66, C70	1.0 nF	L6	100 nH
C5, C10, C15, C25	10 nF	L7	820 nH
C6, C8, C13, C24, C35, C36, C37, C38, C40, C42, C61	100 nF	L9	4.7 µH
C7, C49	100 pF	L10	2.7 µH
C9	2.0 pF	L11	22 nH
C11, C52	33 pF	L12, L13	BLM11B750S
C41	18 pF	Q1, Q2, Q3, Q4, Q5	MMBR941LT1
C12, C20, C47, C54	22 pF	Q6	MMBT3904LT1
C16, C45, D1	Not Used	Q7	MMBT3906LT1
C18, C62	12 pF	R1	6.8 k
C21	0.5 pF	R2	2.2 k
C22	10 pF	R3	2.4 k
C28	47 nF	R4	200
C29, C31, C44	4.7 µF	R5	430
C30	0.1 µF	R6	510
C32	2.2 nF	R7	10
C33	22 nF	R8	8.2 k
C34	3.3 nF	R9	820
C39	10 µF	R10	7.5 k
C48 C50 C67 C69	1.0 µF	R11, R12	10 M
C51, C63	1.0 pF	R13, R14, R15, R16, R17, R20, R21, R22, R25	100 k
C55	15 pF	R18	36 k
C56	56 pF	R19	1.6 k
C64	0.22 µF	R23	24 k
C65	33 nF	R24	9.1 k
C68	2.2 µF	R26	620
D2	MMBV609LT1	R27	1.1 k
FILTER1	SAFC281ME75N	R28	910
FILTER 2	MXF21.4–15A	R29	1.5 k
FILTER3	CFWC450F	U1	MC2800
L1, L8	27 nH	U2	SM5166AV
L2	33 nH	X1	20.945000 MHz

Table 2. SAW Filter Specification

Part Number	SAFC281ME75N [Note]
Nominal Center Frequency, f_O	281.0 MHz
Insertion Loss f_O – 100 MHz to f_O – 37.5 MHz f_O ± 4.0 MHz f_O + 37.5 MHz to f_O + 100 MHz	 48 dB min 4.5 dB max 40 dB min
Ripple within f_O ±4.0 MHz/dB	2.0 max
Nominal Input / Output impedance	230 Ω // – 0.2 pF

NOTE: SAW filter SAFC281ME75N is the product of muRata Manufacturing Co., Ltd. For further enquiry, please refer to the muRata's product catalog.

Table 3. Crystal Filter Specification

Part Number	MXF21.4–15A [Note]
Nominal Center Frequency, f_O	21.400000 MHz ± 1.0 kHz
Number of Pole	2 poles
Pass Band Width	–3.0 dB / ±7.5 kHz min
Stop Band Width	–18 dB / ±25.0 kHz max
Pass Band Ripple	0.5 dB max
Insertion Loss	1.5 dB max
Nominal Input / Output impedance	1.5 kΩ // 2.0 pF

NOTE: Crystal filter MXF21.4–15A is the product of KINSEKI, Ltd. For further enquiry, please refer to the product catalog of Kinseki, Ltd.

Table 4. Ceramic Filter Specification

Part Number	CFWC450F [Note]
Nominal Center Frequency, f_O	450 kHz
6.0 dB Bandwidth from f_O	±6.0 kHz
50 dB Bandwidth from f_O	±12.5 kHz
Stop Band Attenuation Within f_O ± 100 kHz	 50 dB min
Ripple within f_O ± 7.5 kHz	3.0 dB max
Nominal Input/Output impedance	1.5 kΩ

NOTE: Ceramic filter CFWC450F is the product of muRata Manufacturing Co., Ltd. For further inquiry, please refer to muRata's product catalog.

Table 5. Quartz Crystal Specification

Part Number	1U0209450D30F5D0Z [Note]
Nominal Frequency, f_O	20.945 MHz
Holder Type	UM–1
Resonance Mode	Fundamental
Operating Temperature	–30 to 80°C
Frequency Tolerance @ 25°C	±20 ppm
Load Capacitance	30 pF
Equivalent Series Resistance, ESR	30 Ω max
Shunt Capacitance C_0	7.0 pF
Drive Level	0.5 μW
Aging	±5.0 ppm/year

NOTE: The quartz crystals are the products of Hong Kong X'TALS Limited. For further inquiry, please refer to the product catalog of Hong Kong X'TALS Limited or **hkxtals@HongKongCrystal.com**.

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